ELE 448 Lab 7

Due by 01 April, 2020

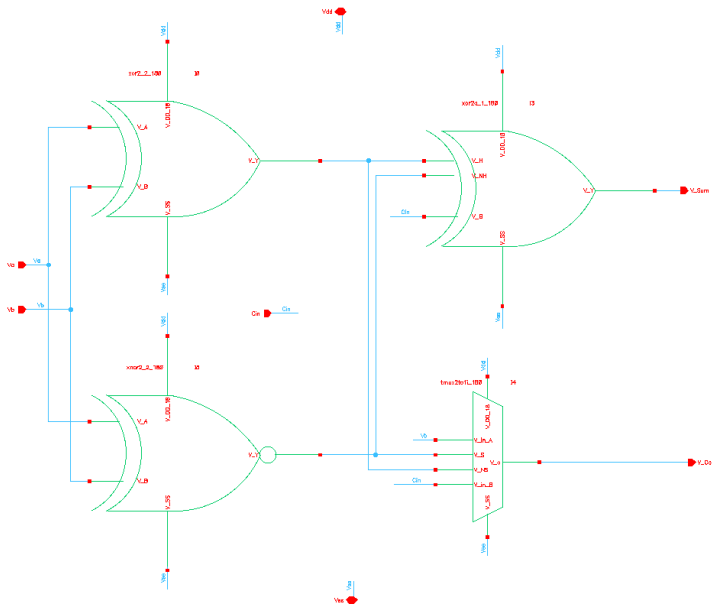
Introduction:

A half adder is defined as an adder that takes two inputs, A and B, and produces two outputs, Sum and Carry. A full adder differs by the fact that it has three inputs, A, B, and $C_{¿}$. If a multi-bit adder is desired, it will require a cascade of full adders; however, the operation on the LSBs can be completed with a half adder. The outputs of a full adder can be constructed from the following logic:

$$S=(A \oplus B) \oplus C_{¿}$$

$$C_{out}=(A \cdot B)+(C_{¿} \cdot (A \oplus B))$$

These logic equations can be implemented by using 2 XORs, a XNOR, and a 2-input multiplexer. The multiplexer works by selecting input A when V_s is high and input B when V_{NS} is high. A 1-bit full adder implemented with these components can be seen below:



Assignments:

1. 1-Bit Full Adder
    a. Create a schematic
    b. Create a symbol
    c. Test the performance
        i. Create a truth table covering all possible input combinations that matches the simulation results

    Questions

    - What are the logic equations for the outputs of a half adder?
    - What signal could replace Vb as the input V_In_A of the multiplexer?

2. 4-Bit Adder
    a. Create a schematic
        i. The carry in pin of the first adder can be connected to ground
        ii. The summation output of each adder will represent one bit of the output signal
        iii. The carry out pin for the first three adders will connect to the carry in pin of its adjacent neighbor
        iv. The carry out pin of the last adder will represent the overflow bit of the output
    b. Create a symbol
    c. Test the performance
        i. Try different combinations of the 4-bit inputs Va and Vb
            1. Show that these combinations produced the corrected outputs by performing the calculations manually